AMENDMENTS TO THE CLAIMS:

1-35. (Canceled)

36. (Previously Amended) The method of claim 37, further comprising forming a second doped well within the first doped region, wherein forming the second doped plug includes forming the second doped plug in the second doped well a second distance from a boundary of the second n-well, and wherein the second distance is selected to provide approximately a desired resistance of a current path between the first doped plug and the second doped plug.

37. (Currently Amended) A method, comprising:

providing a first doped region;

forming a first doped well within the first doped region;

selecting a first distance from a first doped plug to a first boundary of the first doped well to provide approximately a desired breakover voltage between the first doped plug and the first doped region;

forming the first doped plug within the first doped well, wherein the first doped plug is formed the first distance from the first boundary of the first doped well;

forming a second doped plug into the first doped region; and

forming at least one of a LOCOS oxide and a surface trench filled with an oxide ~~an isolation structure~~ between the first and second doped plugs.

38-40. (Cancelled)

41. (Previously Amended) The method of claim 37, further comprising forming a conductor layer above at least a portion of the first and second doped plugs.

42. (Previously Amended) The method of claim 37, wherein providing the first doped region comprises providing a p-type first doped region.

43. (Previously Amended) The method of claim 37, wherein forming the first and second doped plugs comprises forming n-type first and second doped plugs.

44. (Canceled)

45. (Previously Amended) The method of claim 46, further comprising forming a second n-well within the p-type semiconductor substrate, wherein forming the second n-plug within the p-type semiconductor substrate comprises forming the second n-plug within the second n-well a second distance from a boundary of the second n-well, and wherein the second distance is selected to provide approximately a desired resistance of a current path between the first n-plug and the second n-plug.

46. (Currently Amended) A method comprising:

providing a p-type semiconductor substrate;

forming a first n-well within the p-type semiconductor substrate;

selecting a first distance from a first n-plug to a first boundary of the first n-well to provide approximately a desired breakover voltage between the first n-plug and the p-type semiconductor substrate;

forming the first n-plug within the first n-well, wherein the first n-plug is formed the first distance from the first boundary of the first n-well;

forming a second n-plug within the p-type semiconductor substrate; and

forming at least one of a LOCOS oxide and a surface trench filled with an oxide ~~an isolation structure~~ between the first and second n-plugs.

47-48. (Cancelled)

50. (Previously Amended) The method of claim 46, further comprising forming a conductor layer above at least a portion of the first and second n-plugs.

51. (Currently Amended) A method for forming an integrated circuit device, comprising:

providing a semiconductor substrate;

forming a first doped region in the semiconductor substrate;

forming a first doped well within the first doped region;

selecting a first distance from a first doped plug to a first boundary of the first doped well to provide approximately a desired breakover voltage between the first doped plug and the first doped region;

forming the first doped plug within the first doped well, wherein the first doped plug is formed the first distance from the first boundary of the first doped well;

forming a second doped plug within the first doped region;

forming at least one of a LOCOS oxide and a surface trench filled with an oxide ~~an isolation structure~~ between the first and second doped plugs;

forming a bond pad on the semiconductor substrate;

forming a voltage source node on the semiconductor substrate;

coupling the first doped plug to the bond pad;

coupling the second doped plug to the voltage source node; and

forming at least one integrated circuit component on said semiconductor substrate coupled to the bond pad.

52. (Previously Added) The method of claim 51, further comprising forming a second doped well within the first doped region, wherein forming the second doped plug within the first doped region comprises forming the second doped plug within the second doped well.

53. (Cancelled)

54. (Previously Added) The method of clam 51, wherein forming at least one integrated circuit component comprises forming an anti-fuse network.